Exam questions with solutions 2023 - Ionescu

Question 1 (Ionescu):

Single Electron Transistors (SET) are a discrete charge tunneling devices using a conductive nanodot as central island and three other electrodes as source, drain and gate to control the tunneling barriers. Choose the correct properties and characteristics of this device among the following statements.

1. The Coulomb gap in the output characteristics, I_d-V_d, of a SET transistor correspond to the region of drain voltages where the device is in off state; this region of drain voltages is dependent on the applied gate voltage;
2. The same SET device can have both positive and negative transconductance ($g_m=dI_d/dV_g$), depending only on the value of applied gate voltage, at same drain voltage value, therefore one can built a complementary logic using the same device for the equivalent n- and p-type as for instance, building the functionality of an inverter;
3. The background charge effect on SET can affect the periodicity of the SET transfer characteristics.
4. The theoretical R-SET (R=resistive) device, exploiting a stronger electrical potential coupling of the gate to the island, is expected to have increased background charge effect.
5. Under the effect of Coulomb blockade, the transfer characteristics, Id-Vg, of a SET transistor are periodic, with a period equal to e^2/C_Σ, where C_Σ is the total SET capacitance to the ground and e is the elementary charge.
6. If one is using a metallic central island of 1 nm radius surrounded by three metal electrodes (gate, source and drain) with similar radius size, the resulting SET shows Coulomb blockade is expected to be effective at room temperature (T=300K) to build a SET inverter.
7. The intrinsic frequency operation (dictating the speed of the intrinsic device) of a SET can be higher that GHz because of the very fast tunneling processes.
8. An inverter based on two SETs is consuming both static and dynamic power, which is dependent on temperature.
9. One can engineer with controlled strain induced by thermal oxidation silicon gated nanowires to build SET devices without physical oxide barriers between the central island and the drain and source contacts.
10. SETMOS is hybrid equivalent device, made out of a SET and MOSFET achieving high peaks of the current (micro-Amps) with periodic Id-Vg transfer characteristics due to Coulomb blockade.

Question 2 (Ionescu):

Select the correct statements about the semiconducting Tunnel FETs using quantum mechanical band-to-band tunneling conduction mechanisms, from the list below:

1. Tunnel FETs inherit some technology booster (technological parameters that can improve their switch performance) from MOSFETs; among these, one can cite: use of high-k dielectrics, abrupt junctions and thinner semiconducting device bodies.
2. At low voltage and low current levels Tunnel FETs can offer higher analog amplification than MOSFET due to the smaller subthreshold slope.
3. A Tunnel FET with a silicon channel and a germanium source is a heterojunction tunneling device.
4. Trap-Assisted Tunneling (TAT) is a phenomenon that depends on temperature.
5. Trap-Assisted Tunneling (TAT) is a phenomenon that depends on the density of electrically-active traps at both at the tunneling junctions and the oxide-to-channel interfaces.
6. Trap-Assisted Tunneling (TAT) is reduce significantly when the temperature is increasing.
7. Tunnel FET can be used to design more energy efficient hybrid CMOS-TFET multi-core processor architecture. For instance, the computing tasks assigned to Tunnel FETs are the ones requiring high-performance (HP) (faster operation) specifications.
8. The leakage current, I_{off}, of Tunnel FETs decreases at cryogenic (sub-77K) temperatures.
9. In an ideal tunnel FET where the Band-to-Band Tunneling is largely predominant over the trap-Assisted tunneling, the device subthreshold slope is expected to be of 60mV/decade at room temperature (300K).
10. One can build a Single Electron Transistor using Band-to-Band tunneling junctions.